What is claimed is:

1. A III-V compound semiconductor having a layer formed from a first III-V compound semiconductor expressed by the general formula $In_uGa_vAl_wN$ (where $0 \leqq u \leqq 1$, $0 \leqq v \leqq 1$, $0 \leqq w \leqq 1$, $u + v + w = 1$), a pattern formed on said layer from a material different not only from said first III-V compound semiconductor but also from a second III-V compound semiconductor hereinafter described, and a layer formed on said first III-V compound semiconductor and said pattern from said second III-V compound semiconductor expressed by the general formula $In_xGa_yAl_zN$ (where $0 \leqq x \leqq 1$, $0 \leqq y \leqq 1$, $0 \leqq z \leqq 1$, $x + y + z = 1$), wherein the full width at half maximum of the (0004) reflection X-ray rocking curve of said second III-V compound semiconductor is 700 seconds or less regardless of the direction of X-ray incidence.

2. A III-V compound semiconductor having a layer formed from a first III-V compound semiconductor expressed by the general formula $In_uGa_vAl_wN$ (where $0 \leqq u \leqq 1$, $0 \leqq v \leqq 1$, $0 \leqq w \leqq 1$, $u + v + w = 1$), a pattern formed on said layer from a material different not only from said first III-V compound semiconductor but also from a second III-V compound semiconductor hereinafter described, and a layer formed on said first III-V compound semiconductor and said pattern from said second III-V compound semiconductor expressed by the general formula $In_xGa_yAl_zN$ (where $0 \leqq x \leqq 1$, $0 \leqq y \leqq 1$, $0 \leqq z \leqq 1$,

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$x + y + z = 1$), wherein an upper surface of said pattern is not in contact with said second III-V compound semiconductor.

3. A III-V compound semiconductor as set fourth in claim 1 or 2, wherein said pattern is formed from W.

4. A III-V compound semiconductor as set fourth in claim 1 or 2, wherein the first III-V compound semiconductor is expressed by the general formula $In_uGa_vAl_wN$ (where $0 \leqq u \leqq 1$, $0 \leqq v \leqq 1$, $0.01 \leqq w \leqq 1$, $u + v + w = 1$).

5. A III-V compound semiconductor as set fourth in claim 1 or 2, wherein said pattern is a lamination comprising at least two layers which are contacting each other and made of different materials.

6. A III-V compound semiconductor as set fourth in claim 5, wherein said pattern is a lamination comprising at least a layer made of W and a layer made of a material other than W.

7. A III-V compound semiconductor as set fourth in claim 5, wherein said pattern is a lamination comprising at least a layer made of W and a layer made of SiO_2.

8. An electronic device comprising the III-V compound semiconductor as set fourth in claim 1 or 2.

9. A light emitting device comprising the III-V compound semiconductor as set fourth in claim 1 or 2.

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